WHAT IS CLAIMED IS:

1. A buffer memory controller for a hard disk controller, the buffer memory controller comprising:

a data buffer configured to buffer write operation data between a buffer memory and a write head of a disk;

a plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory; and

controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers.

2. The buffer memory controller of Claim 1, further comprising a plurality of block count registers configured to store, for each of the write operations, the corresponding amount of write operation data stored within the buffer memory.

3. The buffer memory controller of Claim 2, wherein the controller logic is further configured to perform the transfers based additionally upon the quantities stored in the block count registers.

4. The buffer memory controller of Claim 3, wherein the block count registers operate as a FIFO.

5. The buffer memory controller of Claim 1, wherein the data buffer operates as a FIFO.

6. The buffer memory controller of Claim 1, wherein the data buffer is configured to supply write operation data to a disk formatter.

7. The buffer memory controller of Claim 1, wherein the address registers operate as a FIFO.

8. The buffer memory controller of Claim 1, wherein the controller logic is further configured to transfer the data of at least two operations based upon a single command to the buffer memory controller.

9. The buffer memory controller of Claim 1, further comprising a busy flag configured to indicate whether the address registers are full.

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10. The buffer memory controller of Claim 1, wherein the number of address registers is at least 4.

11. The buffer memory controller of Claim 1, wherein the number of address registers is at least 8.

12. A method of operating a hard disk unit, the method comprising:

(A) receiving a first write operation;

(B) subsequent to (A), receiving a second write operation;

(C) writing the data of the second write operation to a disk; and

(D) subsequent to (C), writing the data of the first write operation to the disk.

13. The method of Claim 12, further comprising determining that the first write operation and the second write operation write data to the same track.

14. The method of Claim 13, further comprising determining that the second write operation has a lower ending sector number than the starting sector number of the first write operation.

15. The method of Claim 13, further comprising determining that the second write operation is located before the first write operation relative to the position where the write head of the disk is capable of first writing to the track.

16. The method of Claim 13, wherein a portion of the data of the first write operation and a portion of the data of the second write operation are written to the disk during a single revolution.

17. The method of Claim 13, wherein the data of the first write operation and the data of the second write operation are completely written to the disk unit during a single revolution.

18. A method comprising:

receiving a plurality of write operations; and

for each of the write operations, loading a different one of a plurality of address registers of a buffer memory controller with an address within a buffer memory of write operation data of the respective write operation.

19. The method of Claim 18, further comprising, for each of the write operations, loading a different one of a plurality of block count registers of the buffer

memory controller with a value specifying an amount of write operation data associated with the respective write operation.

20. The method of Claim 19, wherein the address registers and the block count registers are loaded with the addresses and amounts of the data of the write operations in the order in which the write operations are to be executed.

21. The method of Claim 18, further comprising, instructing the buffer memory controller to provide the write operation data of the plurality of write operations to a disk formatter.

22. A method of operating a hard disk controller, the method comprising:

loading a first address register of a buffer memory controller with an address in a buffer memory of write operation data of a first write operation; and

loading a second address register of the buffer memory controller with an address in the buffer memory of write operation data of a second write operation,

wherein the first address register is different than the second address register, and wherein the first write operation is different than the second write operation.

23. The method of Claim 22, further comprising instructing, through a single command, the buffer memory controller to provide the write operation data of the first and second write operations to a disk formatter.

24. A method of operating a buffer memory controller of a hard disk controller, the method comprising:

(A) for each of a plurality of write operations, receiving in a different one of a plurality of address registers of the buffer memory controller, an address, within a buffer memory, of write operation data of the respective write operation; and

(B) receiving a command to provide the write operation data of the plurality of write operations.

25. The method of Claim 24, further comprising,

(C) for each of the write operations, receiving in a different one of a plurality of block count registers of the buffer memory controller, a value

specifying an amount of write operation data associated with the respective write operation.

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26. The method of Claim 25, further comprising,

(D) for one of the write operations, transferring write operation data from the buffer memory, the amount of which write operation data is specified by the value in the corresponding block count register and the address of which write operation data is specified by the address in corresponding address register.

27. The method of Claim 26, further comprising, on the buffer memory controller, repeating (D) for each of the remaining write operations.

28. A disk drive controller comprising:

a microprocessor;

a buffer memory for storing write operation data;

a buffer memory controller, the buffer memory controller comprising:

a data buffer configured to buffer write operation data between the buffer memory and a write head of a disk;

a plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory; and

controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers; and

firmware code that is executed by the microprocessor, the firmware code configured to enable the microprocessor perform write operations in an order other than the order in which the write operations are received by the controller.

29. The disk drive controller of Claim 28, wherein the firmware code is configured to cause the microprocessor to:

(A) identify a first write operation received by the controller;

(B) identify a second write operation received by the controller after the first write operation;

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(C) load a first of the address registers of the buffer memory controller with an address in the buffer memory of the write operation data of the second write operation;

(D) load a second of the of the address registers of the buffer memory controller with an address in the buffer memory of the write operation data of the first write operation; and

(E) issue a single command to the buffer memory controller that causes the buffer memory controller to transfer the data identified by the first address register and subsequently transfer the data identified by the second address register.